Post-fabrication soft trimming of resistive sensors
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1. Abstract
A compact and efficient architecture is introduced as an alternative to laser-trimmed precision thin-film resistor. The purpose is to compensate for process-induced offset in Wheatstone bridges and to avoid the then-obtained degradation in terms of full-scale, non-linearity, power supply noise rejection... Expected advantages are a reduced cost due to the fully-electrical implementation and, depending on the programming technology, a possible recalibration of high-end sensors.

Keywords: MEMS, Resistive sensor, Trimming, Offset cancellation, Temperature drift reduction, PSRR.

2. Introduction
In these days the MEMS resistive sensors have become widely used in many applications like medical, army, avionics ... etc. Their classic architecture is based on the Wheatstone bridge. They are generally simple to design and their realization is inexpensive. However, they have many defects like: offset due to manufacturing, sensitivity not adapted to the measuring device, temperature drift, and power supply noise rejection.

The aim of this paper is to propose a passive conditioning circuit consisting of digital potentiometers which can be controlled manually or automatically.

3. Wheatstone bridge limitations in presence of PVT variations
Let’s consider a resistive sensor where the sensitive resistances are placed in a Wheatstone Bridge (WB) as depicted in Figure 1.a. According to the different types of sensors, one up to four of the resistances may vary with the physical signal while the others have fixed values. Some non-exhaustive examples are:

- Sensors with a single sensitive element: $R_{1-} = R_{2-} = R_{2+} = R_0$; $R_{1+} = R_0 + \Delta R$
- Differential sensors: $R_{1-} = R_{2+} = R_0$; $R_{1+} = R_0 + \Delta R$; $R_{2-} = R_0 - \Delta R$
- Full bridge: $R_{2+} = R_{1+} = R_0 + \Delta R$; $R_{1-} = R_{2-} = R_0 - \Delta R$

Where $R_0$ is the nominal value of all resistors and $\Delta R$ is the variation of the sensing resistances induced by the physical magnitude to be measured.

The differential output voltage then relates to the supply voltage applied across the bridge ($V_{dd}$) and to the relative variation of resistances as in:

$$V_{out} = V_{o+} - V_{o-} = \alpha V_{dd} \frac{\Delta R}{4R_0} \quad (1)$$
Where \( \alpha \) is the number of sensitive resistors in the bridge, i.e. 1, 2 or 4. Advantages of such an arrangement with respect to the rejection of power supply noise (PSRR) or temperature effects are well known for many years.

![Figure 1: a) Wheatstone bridge arrangement of a resistive sensor (left) – b) Wheatstone bridge connection to the « soft » trimming ASIC (right).](image)

However, mismatches due to fabrication processes lead to an unbalanced bridge even in the absence of input signal. Figure 2.a illustrates the offset obtained using Monte-Carlo (MC) simulations on a WB with integrated resistors \( R_o = 5k\Omega \). Under a 5V power supply, a maximum offset of 18mV is obtained that corresponds to a “signal”, i.e. a variation of resistance, of 0.36% for a full bridge or 1.44% for a WB with a single sensitive element. Even if this offset lies in the specification, it induces the degradation of the PSRR as illustrated by Figure 2.b and in the worst case a PSRR as low as 48dB may be obtained. For small variations of the sensor resistances, the output differential signal can be very small, typically \( \mu \)V for ppm variations and thus, the signal will be lower than the offset and PSSR may limit the resolution, i.e. the minimum variation of resistance that may be detected.

![Figure 2: Effect of mismatches at the output of a Wheatstone bridge: (a) Offset in mV and (b) Power Supply Rejection Ratio in db.](image)

In that case, state of the art solutions consist in using laser trimming to balance the bridge after fabrication, generally using an external set of trimming resistors [1] or smart front-ends [2]. The first solution requires an additional die and a laser trimmer for an expensive calibration procedure while the second transforms a passive sensor in an active one and limits the bandwidth in low frequencies. The proposed architecture allows an electrical only calibration procedure with an apparently passive WB approach.

**4. Proposed architecture**

The proposed solution consists in connecting the sensor resistors to a calibration ASIC as depicted in Figure 1.b. As a result, the CMOS die and the sensor are packaged as a single device with four external I/O (namely \( V_{o+}, V_{o-}, V_{dd} \) and \( V_{ss} \)) while few control inputs are used during post-fabrication calibration. The first idea to compensate for the process-induced offset is to connect a digital potentiometer between \( V_{dd} \) and both terminals of the WB as depicted in Figure 3. As an example, if the maximum offset to be compensated is equivalent to 1.5% of \( R_o \), and if this resistance is discretized in 7 elements (\( n=7 \)), then \( R_{os} \) will be equal to 0.21% of \( R_o \) and the obtained offset should be reduced by at least half order of magnitude. There are different ways for controlling the \( n+1 \) switch to compensate for the post-
fabrication offset. The calibration procedure presented hereafter is minimizing the impact of the on-state resistance of MOS transistors and easy to implement:

**Objective**: Initially, all transistors are in the on-state and \( V_{o+} - V_{o-} \) is measured, while a zero physical input is applied to the sensor. If the differential output is positive (respectively negative) a resistance must be serially added to \( R_{1_-} \) (resp. \( R_{1_+} \)) that is connected to \( V_{b1} \) (resp. \( V_{b2} \)).

**Procedure**: First, the transistor controlled by \( C_0 \) (resp. \( C_n \)) is opened to add \( R_{os1} \) (resp. \( R_{osn} \)) in series with \( R_{1_-} \) (resp. \( R_{1_+} \)). If the offset sign does not change at this step, proceed in opening the switches from left to right (resp. right to left) till the offset sign changes: then the point that gives the best offset can be manually chosen between the first before the offset sign changes and the second after the sign changes.

![Wheatstone Bridge (from Figure 1.a)](image)

The final configuration is then the configuration that compensates for the post-fabrication offset. The total number of configurations is obviously equal to \( 2^n \). In the example above 4 bits are necessary to encode all configurations (\( n=7 \)). At this stage a MC simulation can be performed to verify the efficiency in improving both offset and PSRR. Results reported in table1 show a reduction of the maximum offset by a factor of 13 and a reduction of its standard deviation from 5.7 mV down to 790 µV. PSRR is also improved as the minimum PSRR is increased from 48dB up to 70.5dB with 7 resistors in the digital potentiometer. Obviously, increasing the number of elementary resistors may increase performance.

However, it is not possible to expect the temperature coefficients of both kinds of resistors, fabricated in different technologies, to be identical. As a result, (see figure5-a), the offset temperature coefficient of the so-obtained WB is responsible of sensor offset drifting. This point is addressed in the next section.

<table>
<thead>
<tr>
<th>Monte-Carlo Results</th>
<th>Min</th>
<th>Max</th>
<th>Mean</th>
<th>Std-dev</th>
</tr>
</thead>
<tbody>
<tr>
<td>Offset (mV)</td>
<td>-1.4</td>
<td>1.4</td>
<td>0.016</td>
<td>0.790</td>
</tr>
<tr>
<td>PSSR (dB)</td>
<td>70.5</td>
<td>118</td>
<td>80.5</td>
<td>9.5</td>
</tr>
</tbody>
</table>

*Table 1 PSSR and Offset after coarse tuning with 7 elementary resistors.*
5. Cancellation of temperature effects
Starting from the maximum offset induced by process variations, i.e. 18 mV, a series resistance $R_s$ corresponding to 1.44\% of the sensor resistance, is connected between $V_{B2}$ (see Figure 1.a) and $V_{dd}$. As a result, offset is cancelled at ambient temperature (27°C) but a thermal drift of about 65μV/°C is observed (Figure 5.a) and offset ranges from 3.5mV down to -3mV over the -20°C up to 80°C temperature range.

The technique of temperature effect compensation is described in literature [3]. To summarize, a resistance $R_p$ is added in parallel with $R_{2-}$ (see Figure 1.a) and a calculation shows that the so-obtained temperature coefficient for the right-side half bridge is null if:

$$R_s R_p = R_{1+} R_{2-} \approx R_0^2$$

Where $R_s$ and $R_{2-}$ have the same temperature coefficient and are fabricated in the same process. In addition, TCR of these resistances must be as low as possible to avoid 2nd order effects of temperature.

6. Improved architecture
To implement the technique of offset compensation presented in section 4, two digital linear potentiometers R2R are added in parallel of $R_{2+}$ and $R_{2-}$ (figure 4).

According to equation (2) when $R_s$ is very small then $R_p$ is very large, and a nonlinear relation between $R_s$ and $R_p$ can be noticed. The solution to have an almost linear variation of $R_{op}$ with $R_{os}$ is to add two serial resistors $R$ equal to 100$R_{os}$ with $R_{os1}$ (resp. $R_{osn}$).

$$R_p = n R_{op} \approx \frac{R_0^2}{R + n R_{os}}$$

**Procedure**: when $R_{os1}$ is added (resp. $R_{osn}$) in series with $V_{B1}$ (resp. $V_{B2}$) one $R_{op}$ have to be removed from left (resp. from right); this procedure is repeated until the offset sign changes. This stage is called as offset coarse tuning and temperature drift reduction.
As a result, a thermal drift of 2.4μV/°C is observed on Figure 5.b and offset ranges from 1.08mV down to 0.84mV over the -20 °C up to 80 °C temperature range. Then, the impact of the temperature is almost eliminated.

Note: adding resistors in series and in parallel with the sensing resistors decreases the sensor sensitivity. It was assumed that the sensor has a higher sensitivity than required. Anyway, an amplifier with adjustable gain is recommended to increase the sensitivity.

7. **Automatic fine calibration**

In addition to the offset compensation solution previously presented, an automatic offset calibration procedure is proposed to compensate for the remaining offset and to ensure the sensor long life. This automatic procedure uses a comparator to determine offset sign (positive or negative). At each start-up, a finite-state machine controlled by the comparator sign sweeps all possible combinations and stops when offset sign is changing.

Note that RF resistors values are very small in front of the $R_{OS}$ resistors; basically $R_{OS} = \sum R_F$. Therefore, the temperature impact in this stage is ignored. Moreover, a comparator with very low offset and thermal drift has to be designed.

The previous remaining maximum offset after the coarse tuning was +/-1.4mV (see table1). Therefore, using $7R_F$ resistors (controlled by 4 bits), a maximum final offset equal to +/- 200μV could be obtained with an ideal comparator.
Finally, due to the offset comparator, the final results reported in figure 6 show a final offset between +/-500µV with a standard deviation reduced from 790 µV down to 212µV. PSRR is also improved since the minimum PSRR is increased from 70.5dB up to 77dB.

8. Sensitivity adjustment

The sensor sensitivity depends on the supply voltage and the bridge resistance $R_0$, even if $\Delta R/R_0$ is independent of $R_0$. In general, and according to the application, sensors have a sensitivity specification to respect. Then, if its initial value is higher than this requirement, it can be adjusted by using two potentiometers $R_{VSS}$ and $R_{VDD}$ as shown in Figure 4. To keep the output common mode at the value of $V_{DD}/2$, these potentiometers are controlled symmetrically. An example is shown in Figure 7 where both values of $R_{VSS}$ and $R_{VDD}$ are increased from 0 to 2.5kΩ with 5 control bits and a step of 80Ω. Therefore, the suitable sensitivity can be adjusted for the application in keeping the common mode at $V_{DD}/2$ and the adjustment resolution depends on the number of control bits of $R_{VSS}$ and $R_{VDD}$.
9. Conclusion

In this paper, a passive post-fabrication soft trimming architecture is proposed to improve the power supply noise rejection ratio (PSRR), the offset cancellation, the thermal drift reduction and sensitivity adjustment of a Wheatstone bridge.

For this purpose, two offset tunings are used in the first design of an ASIC; the first one, called coarse tuning, is controlled manually but it could be automatically controlled in the future, and the second one, called fine tuning, is controlled automatically with a comparator and a state machine.

This architecture is applicable to all resistive sensors based on a Wheatstone bridge.

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References

